Data Sheet | July 23, 2007 | FN9083.3

Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6520B makes simple work out of implementing a complete control scheme for a DC/DC stepdown converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, the ISL6520B integrates the control, output adjustment and monitoring functions into a single 8 Lead package.

The ISL6520B provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±1.5% over-temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

The error amplifier features a 15MHz gain-bandwidth product and 8V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6520BCB*	6520 BCB	0 to +70	8 Ld SOIC	M8.15
ISL6520BCBZ* (Note)	6520 BCBZ	0 to +70	8 Ld SOIC (Pb-free)	M8.15
ISL6520BCR*	65 20BCR	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6520BCRZ* (Note)	65 20BCRZ	0 to +70	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6520BIR*	65 20BIR	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL6520BIRZ* (Note)	65 20BIRZ	-40 to +85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6520EVAL1	Evaluation Board			

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

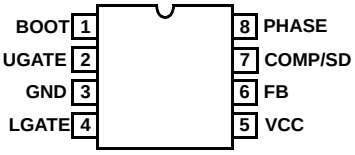
- Operates from +5V Input
- 0.8V to V_{IN} Output Range
  - 0.8V Internal Reference
  - ±1.5% Over Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Cycle
- Small Converter Size
  - 300kHz Fixed Frequency Oscillator
  - Internal Soft Start
  - 8 Ld SOIC or 16Ld 4mmx4mm QFN
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free Plus Anneal Available (RoHS compliant)

Applications

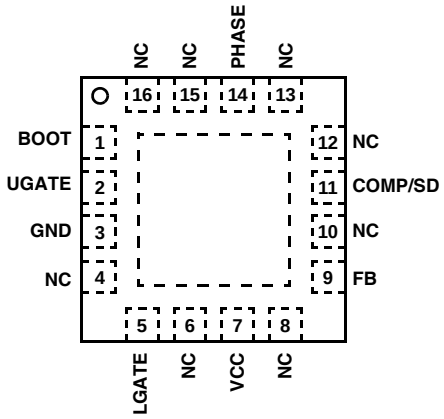
- Power Supplies for Microprocessors
  - PCs
  - Embedded Controllers
- Subsystem Power Supplies
  - PCI/AGP/GTL+ Buses
  - ACPI Power Control
  - SSTL-2 and DDR SDRAM Bus Termination Supply
- Cable Modems, Set-Top Boxes, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC/DC Regulators
- Low-Voltage Distributed Power Supplies

Pinouts

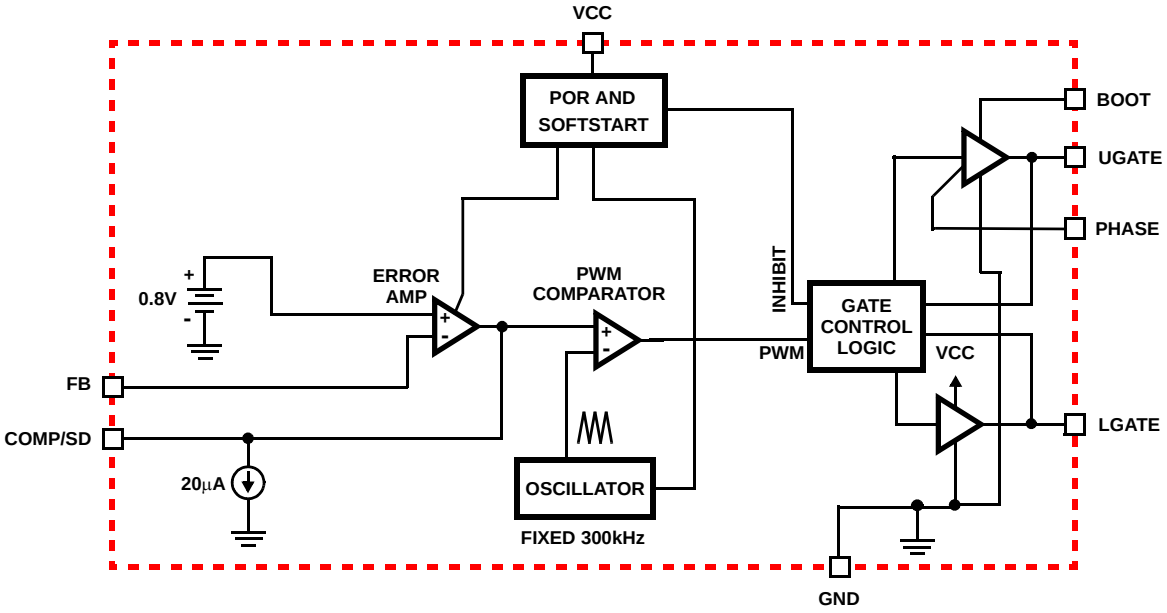
ISL6520B
(8 LD SOIC)
TOP VIEW



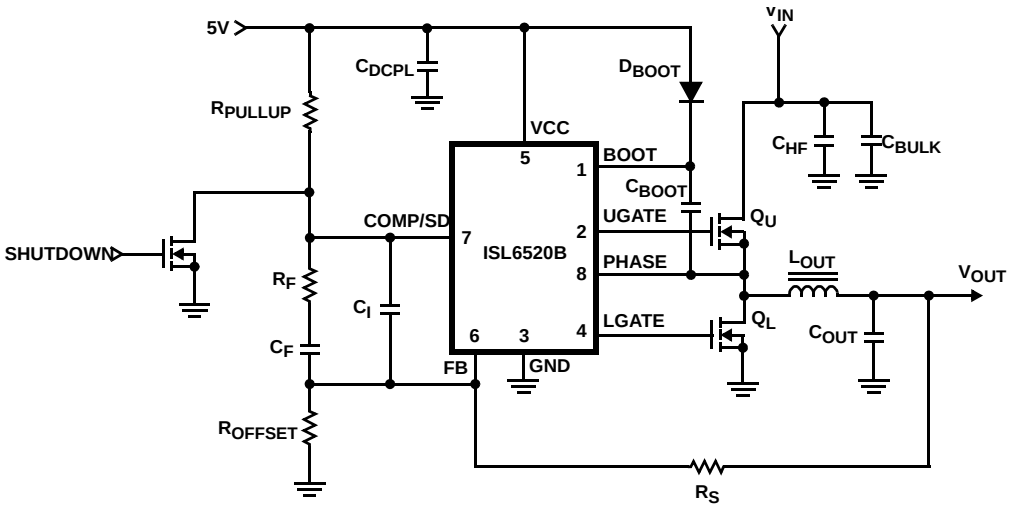
ISL6520B
(16 LD QFN)
TOP VIEW



Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +6.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +15.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . 7.0V (DC)
8.0V (<10ns Pulse Width, 10µJ)
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, VCC . . . . . +5V ±10%
Ambient Temperature Range - ISL6520BC . . . . . 0°C to +70°C
Junction Temperature Range. . . . . .-40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
QFN Package (Notes 2, 3).	45	7

Maximum Junction Temperature
(Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{VCC}		2.6	3.2	3.8	mA
POWER-ON RESET						
Rising VCC POR Threshold	POR		4.19	4.30	4.50	V
VCC POR Threshold Hysteresis			-	0.25	-	V
OSCILLATOR						
Frequency	f_{OSC}	ISL6520BC, VCC = 5V	250	300	340	kHz
		ISL6520BI, VCC = 5V	230	300	340	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance		ISL6520BC	-1.5	-	+1.5	%
		ISL6520BI	-2.5		+2.5	%
Nominal Reference Voltage	V_{REF}		-	0.800	-	V
ERROR AMPLIFIER						
DC Gain		(Note 4)	-	88	-	dB
Gain-Bandwidth Product	GBWP	(Note 4)	-	15	-	MHz
Slew Rate	SR	(Note 4)	-	8	-	V/µs
GATE DRIVERS						
Upper Gate Source Current	$I_{UGATE-SRC}$	V_{BOOT} - V_{PHASE} = 5V, V_{UGATE} = 4V	-	-1	-	A
Upper Gate Sink Current	$I_{UGATE-SNK}$		-	1	-	A
Lower Gate Source Current	$I_{LGATE-SRC}$	V_{VCC} = 5V, V_{LGATE} = 4V	-	-1	-	A
Lower Gate Sink Current	$I_{LGATE-SNK}$		-	2	-	A
DISABLE						
Disable Threshold	$V_{DISABLE}$		-	0.8	-	V

NOTE:

4. Limits should be considered typical and are not production tested

Functional Pin Description

VCC

This pin provides the bias supply for the ISL6520B, as well as the lower MOSFET's gate. Connect a well-decoupled 5V supply to this pin.

FB

This pin is the inverting input of the internal error amplifier. Use this pin, in combination with the COMP/SD pin, to compensate the voltage-control feedback loop of the converter.

GND

This pin represents the signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available.

PHASE

Connect this pin to the upper MOSFET's source.

UGATE

Connect this pin to the upper MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

BOOT

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-channel MOSFET.

COMP/SD

This pin is the output of the error amplifier. Use this pin, in combination with the FB pin, to compensate the voltage-control feedback loop of the converter.

Pulling COMP/SD to a level below 0.8V disables the controller. Disabling the ISL6520B causes the oscillator to stop, the LGATE and UGATE outputs to be held low, and the softstart circuitry to re-arm. The COMP/SD pin must be pulled above 0.8V to terminate shutdown. This may be done through a pullup resistor tied between VCC and COMP/SD. The recommended range of resistor values to use as the pullup resistor is between 50kΩ and 100kΩ.

LGATE

Connect this pin to the lower MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

Functional Description

Initialization

The ISL6520B automatically initializes upon receipt of power. The Power-On Reset (POR) function continually monitors the bias voltage at the VCC pin. The POR function initiates the soft start operation.

Soft Start

The ISL6520B is held in reset with both UGATE and LGATE driven to ground until the POR threshold on VCC has been reached and the COMP/SD pin has been pulled above 0.8V. If COMP is not actively pulled high following POR the internal 20μA current sink will hold COMP/SD low and the device will remain in reset. COMP/SD can either be statically tied to VCC through a pullup resistor or driven high through a resistor to terminate reset. The recommended range of resistor values to use as the pullup resistor is between 50kΩ and 100kΩ.

Following reset the ISL6520B provides a 1024 clock cycle settling period (~3.4ms) prior to initiating softstart. At the conclusion of the settling period the COMP/SD pin is driven to 0.8V for 24 clock cycles (~75μs) to discharge the compensation network. Soft start of the regulated output is generated by imposing an internal offset on the FB pin which ramps down from 0.8V to 0V over the next 2048 clock cycles (~6.8ms). Total time from end of reset to completion of soft-start is 10.2ms.

Pulling COMP/SD below 0.8V or VCC dropping below minimum POR initiates another reset.

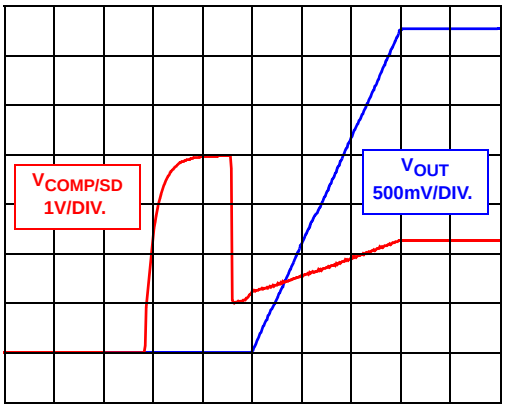


FIGURE 1. SOFT START INTERVAL

Current Sinking

The ISL6520B incorporates a MOSFET shoot-through protection method which allows a converter to sink current as well as source current. Care should be exercised when designing a converter with the ISL6520B when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating it's input voltage. This means that the converter is boosting current into the V_{CC}

rail, which supplies the bias voltage to the ISL6520B. If there is nowhere for this current to go, such as to other distributed loads on the V_{CC} rail, through a voltage limiting protection device, or other methods, the capacitance on the V_{CC} bus will absorb the current. This situation will allow voltage level of the V_{CC} rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of the ISL6520B, then the IC will experience an irreversible failure and the converter will no longer be operational. Ensuring that there is a path for the current to follow other than the capacitance on the rail will prevent this failure mode.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

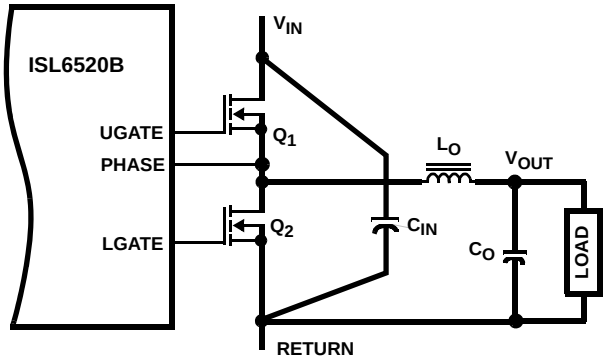


FIGURE 2. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 2 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. The components shown in Figure 2 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O may each represent numerous physical capacitors. Locate the ISL6520B within 3 inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the ISL6520B must be sized to handle up to 1A peak current.

Figure 3 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the COMP/SD pin and locate the resistor, R_{OSCET} close to the COMP/SD pin because the internal current source is only 20µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins. All components used for feedback compensation should be located as close to the IC a practical.

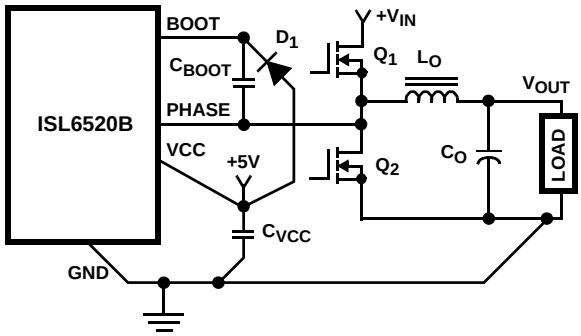


FIGURE 3. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Feedback Compensation

Figure 4 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

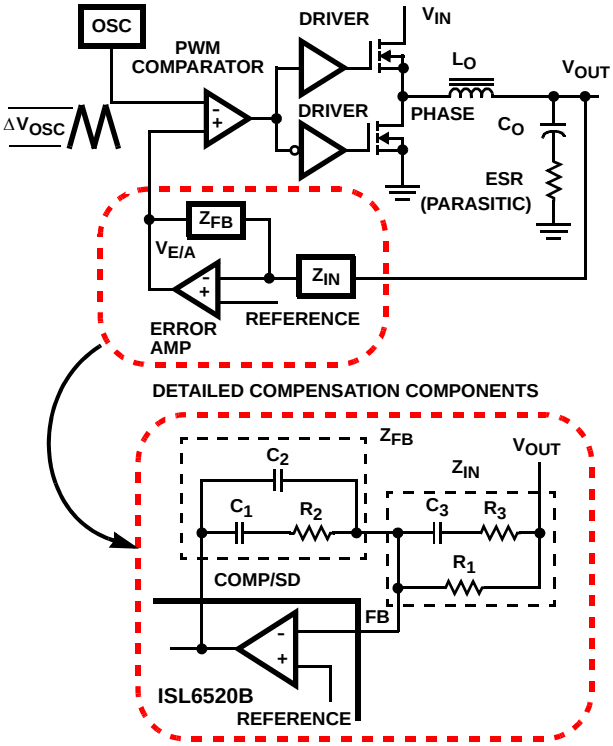


FIGURE 4. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad f_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(EQ. 1)}$$

The compensation network consists of the error amplifier (internal to the ISL6520B) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 4. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \quad \text{(EQ. 2)}$$

Figure 5 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 5. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 5 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

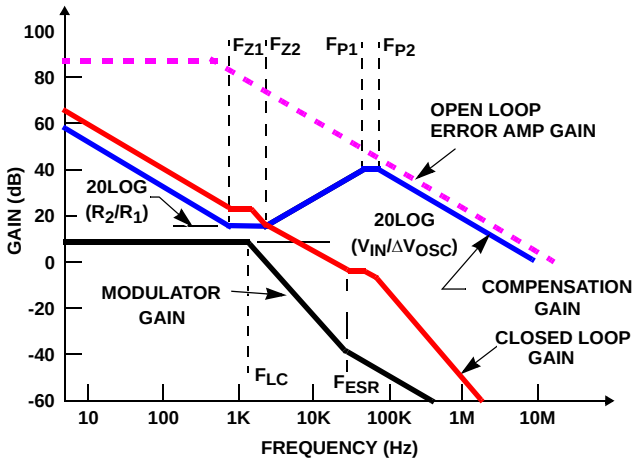


FIGURE 5. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 3)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6520B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 4)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge currentrating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6520B requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6520B and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Losses while Sourcing Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Losses while Sinking Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the combined switch ON and OFF time, and
F_S is the switching frequency.

(EQ. 5)

Given the reduced available gate bias voltage (5V), logic-level or sub-logic-level transistors should be used for both N-MOSFETs. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-

through protection present aboard the ISL6520B may be circumvented by these MOSFETs if they have large parasitic impedences and/or capacitances that would inhibit the gate of the MOSFET from being discharged below it's threshold level before the complementary MOSFET is turned on.

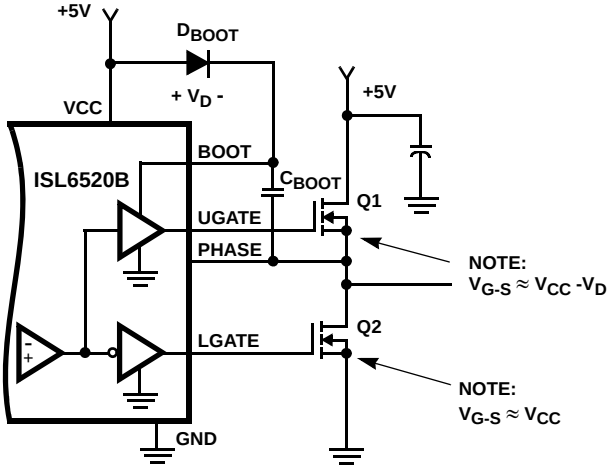
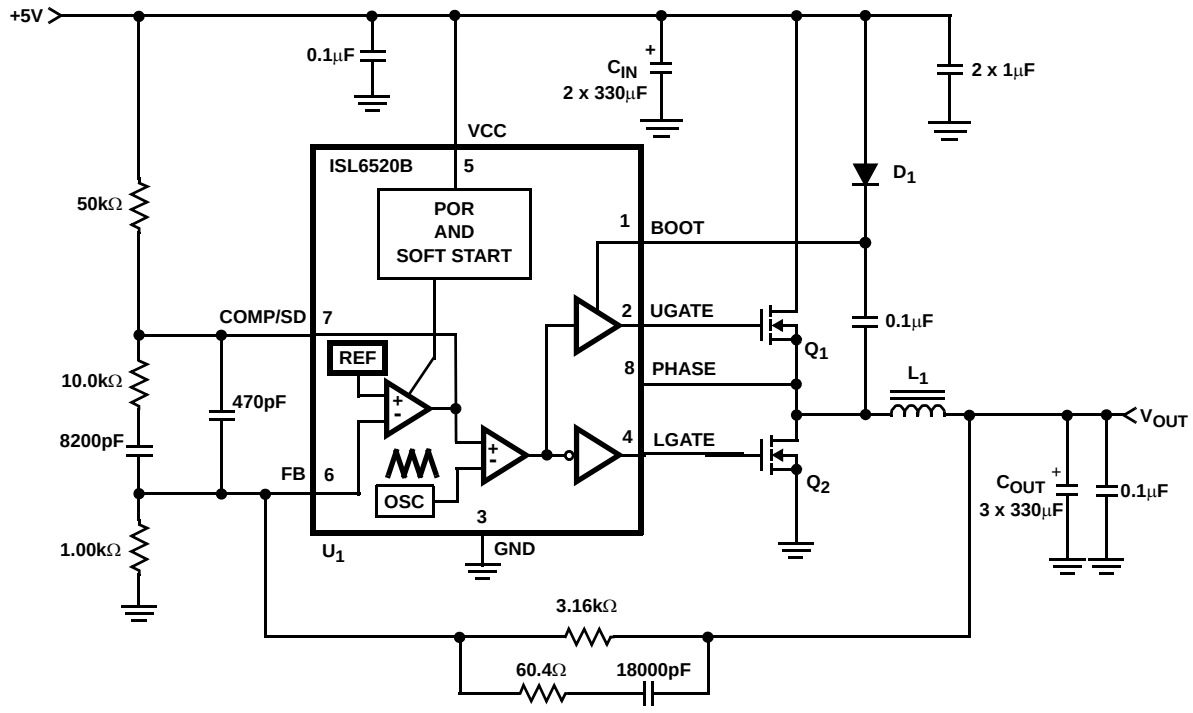


FIGURE 6. UPPER GATE DRIVE BOOTSTRAP

Figure 6 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. The supply is refreshed to a voltage of V_{CC} less the boot diode drop (V_D) each time the lower MOSFET, Q_2, turns on.

ISL6520B DC/DC Converter Application Circuit

Figure 7 shows an application circuit of a DC/DC Converter. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN9932.

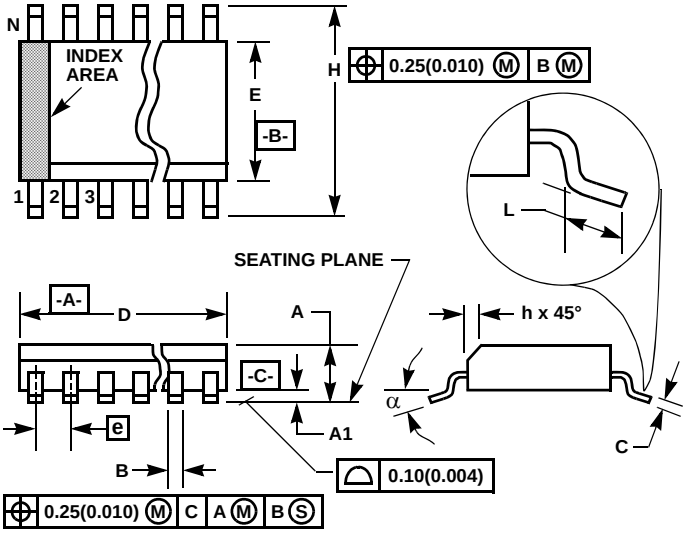


Component Selection Notes:

C_{IN} - Each 330mF 6.3WVDC, Sanyo 6TPB330M or Equivalent.
C_{OUT} - Each 330mF 6.3WVDC, Sanyo 6TPB330M or Equivalent.
D1 - 30mA Schottky Diode, MA732 or Equivalent
L_1 - 3.1µH Inductor, Panasonic P/N ETQ-P6F2ROLFA or Equivalent.
Q_1, Q_2 - Fairchild MOSFET; HUF76143.

FIGURE 7. 5V TO 3.3V 15A DC/DC CONVERTER

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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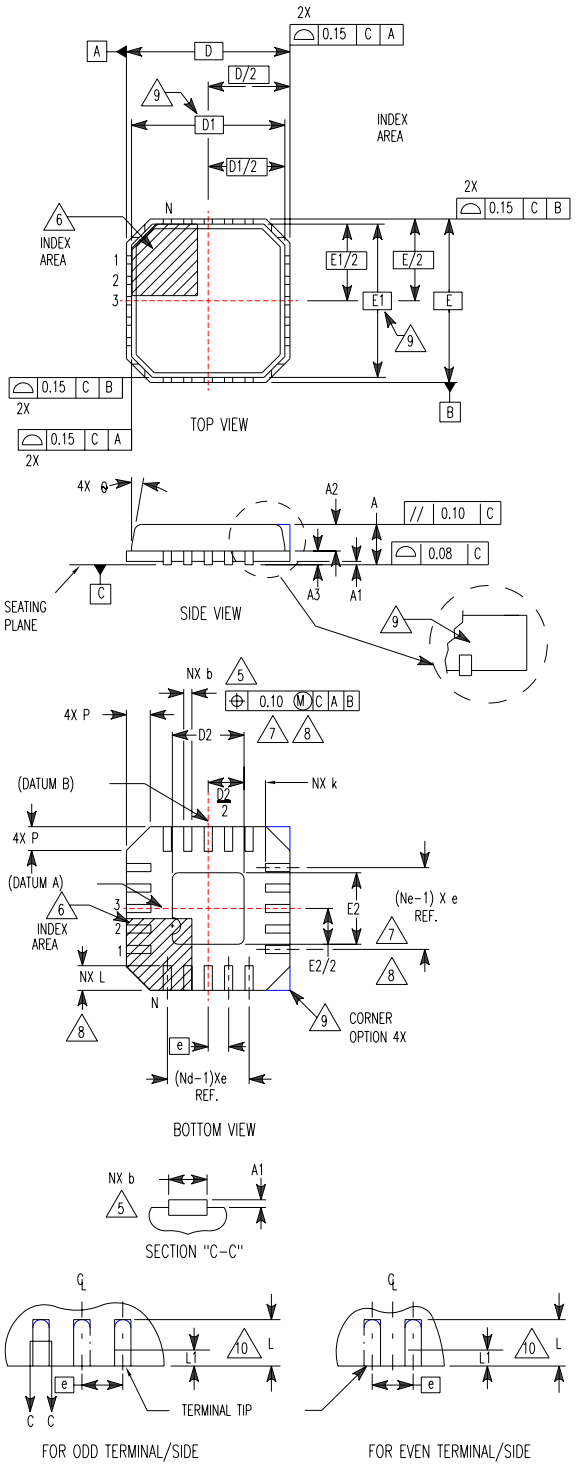
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.